IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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06/26/2007 /Pamela Gerik/
Date Pamela Gerik

APPEAL BRIEF

Sir/Madam:

Further to the Notice of Appeal filed April 26, 2007, Appellant presents this Appeal Brief. The Notice of Appeal was filed following receipt of a final Office Action mailed December 13, 2006. Appellant hereby appeals to the Board of Patent Appeals and Interferences from the rejection of pending claims 10-23, and respectfully requests that this appeal be considered by the Board.

I. REAL PARTY IN INTEREST

The subject application is owned by LSI Logic Corporation having a place of business at 1621 Barber Lane, Milpitas, California 95035.

II. RELATED APPEALS AND INTERFERENCES

No appeals, interferences, or judicial proceedings are known which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-9, 24, and 25 are canceled. Pending claims 10-23 stand rejected and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

No amendments to the claims were filed subsequent to their final rejection. Therefore, the Appendix hereto reflects the current state of the claims.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 10 recites a telephony signaling circuit, comprising: a comparison register adapted to store first signal bits contained within a first data sequence received over a voice channel (Specification -- pg. 15, lines 24-25; pg. 16, lines 10-15; pg. 26, lines 18-20); and a comparator adapted to compare the first signal bits stored in the comparison register against second signal bits contained within a second data sequence received over the voice channel and, if the first signal bits differ from the second signal bits, to replace the first signal bits stored in the comparison register with the second signal bits and to notify a digital signal processor coupled to the comparator of the replacement (Specification -- pg. 15, lines 26-30; pg. 16, lines 10-15; pg. 26, line 20 – pg. 27, line 5).

Independent claim 18 recites a method for detecting telephony signals, comprising: storing in a comparison register first signal bits contained within a first data sequence received over an input voice channel (Specification -- pg. 15, lines 24-25; pg. 16, lines 10-12; pg. 26, lines 18-20); comparing the first signal bits against second signal bits contained in a second data sequence received over the input voice channel (Specification -- pg. 15, lines 26-30; pg. 16, lines 12-15; pg. 26, lines 20-22); and if the first signal bits differ from the second signal bits, replacing the first signal bits with the second signal bits (Specification -- pg. 15, lines 26-30; pg. 16, lines 12-15; pg. 26, line 23 – pg. 27, line 5).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 10 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over various combinations of U.S. Patent No. 5,144,624 to Sharper et al. (hereinafter "Sharper") and U.S. Patent No. 4,893,310 to Robertson et al. (hereinafter "Robertson").

2. Claims 11-17 and 19-22 [sic] stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sharper, Robertson, and U.S. Patent No. 6,782,066 to Nicholas et al. (hereinafter "Nicholas").

VII. ARGUMENT

The contentions of the Appellant with respect to the ground of rejection presented for review, and the basis thereof, with citations of the statutes, regulations, authorities, and parts of the record relied upon are presented herein for consideration by the Board. Details as to why the rejections cannot be sustained are set forth below.

Rejection of Claims 10 and 18

Claims 10 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over various combinations of U.S. Patent No. 5,144,624 to Sharper et al. (hereinafter "Sharper") and U.S. Patent No. 4,893,310 to Robertson et al. (hereinafter "Robertson"). To establish a case of *prima facie* obviousness of a claimed invention, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Second, there must be a reasonable expectation of success. As stated in MPEP 2143.01, the fact that references can be hypothetically combined or modified is not sufficient to establish a *prima facie* case of obviousness. *See In re Mills*, 916 F.2d. 680 (Fed. Cir. 1990). Finally, the prior art references must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d. 981 (CCPA 1974); MPEP 2143.03. Specifically, "all words in a claim must be considered when judging the patentability of that claim against the prior art." *In re Wilson* 424 F.2d., 1382 (CCPA 1970).

In response to the recent U.S. Supreme Court decision in *KSR Int'l Co. v. Teleflex, Inc.* (U.S. 2007), new guidelines were set forth for examining obviousness under 35 U.S.C. § 103. The U.S. Supreme Court reaffirmed the *Graham* factors and, while not totally rejecting the "teachings, suggestion, or motivation" test, the Court appears to now require higher scrutiny on the part of the U.S. Patent & Trademark Office. In accordance with the recently submitted guidelines, it is "now necessary to identify the reason" why a person of ordinary skill in the art would have combined the prior art elements in the manner presently claimed. Moreover, even if combined, the *Graham* factors require that a determination of the differences between the combined prior art and the claims at issue is needed. Using these standards, Applicant contends that the cited art fails to teach or suggest all features of the currently pending claims, some distinctive features of which are set forth in more detail below.

The combination of Sharper and Roberson do not teach or suggest a comparator that replaces first signal bits within a first data sequence with second signal bits within a second data sequence if the first signal bits differ from the second signal bits. Present independent claims 10 and 18 each describe a comparator or "comparing" step. The comparator or comparing step compares first signal bits within a first data sequence with second signal bits within a second data sequence. If the result of that comparison yields a difference between the first signal bits and the second signal bits, then the first signal bits are replaced by the second signal bits. Replacement occurs by substituting the second bits into the locations of the first signal bits contained within the first data sequence. In this manner, the signal bits are constantly updated, but only if a change occurs. If the comparison does not yield a difference, then replacement does not occur and the digital signal processor is not notified through an interrupt or any other processing stall functionality.

Contrary to independent claims 10 and 18, it is impossible for Sharper or Robertson to perform any replacement whatsoever. Instead, Sharper describes two modes of operation. The first mode deals specifically with detecting a signaling bit, and second mode deals with restoring a signaling bit. As to the first mode, the reason a signaling bit must be detected is to indicate a system mode. Specifically, the state of a signaling bit can be interpreted to indicate an "on-hook," "off-hook," or "maintenance" system mode (Sharper -- col. 1, lines 51-61). The eighth

bit of each frame within a super frame carries the signaling bit, and the digital switch 23 or 32 (Sharper -- Fig. 1) imparts the signaling bit. A logic 1 in the eighth bit of every frame connotes an "off-hook" system mode, alternating logic 1's and 0's connotes a "maintenance" system mode, and a logic 0 in the eight bit position of every sixth frame connotes an "on-hook" system mode. In order to know which CPE1 or CPE2 is sending information across the truck lines 11 and 15 (Sharper -- Fig. 1), it is necessary to detect the signaling bit at the eighth bit location of every frame or in every sixth frame (Sharper -- col. 5, lines 36-57).

Sharper describes a signaling bit detection circuit 100 (Sharper -- Fig. 4). Circuit 100 includes a shift register 142 that selects only the eighth bit of each byte per frame (Sharper -- col. 5, lines 65-67). A comparator 45 compares the eighth bit of frames that are six frames apart (Sharper -- col. 6, lines 11-14). If the eighth bit of each byte is a logic 0, indicating an "on-hook" system mode, then comparator 45 will indicate a logic 0 output, for example (Sharper -- col. 6, lines 12-16). Detection circuit 100 is used to detect a system mode, however, if the frames are somehow misaligned, then the detection circuit and the corresponding system mode provided to the recipient CPE will be incorrect (Sharper -- col. 2, lines 13-27). Accordingly, it is necessary to correct or "restore" the signaling bit to what is known as a pre-converted state in order to keep the frames aligned (Sharper -- col. 2, lines 41-49; col. 3, lines 19-23). Thus, the restoration circuit 110 is needed.

Restoration circuit 110 utilizes a comparator 70 that compares the Xth (e.g., eighth) bit of a frame arriving across line 40 with the Xth bit of a frame W frames earlier, and with the Xth bit of a frame Z frames earlier (i.e., W = 2; Z = 4) (Sharper -- col. 3, lines 31-33). If the Xth bit was converted, restoration circuit 110 restores the Xth bit to its pre-converted state (Sharper -- col. 3, lines 34-36). While no reasons were given by the Examiner as to why the above statement renders independent claims 10 and 18 obvious, Appellant will explain in the context of Sharper why claims 10 and 18 are non-obvious.

The operation of restore circuit 110 is best illustrated beginning in column 7, line 48, in conjunction with Fig. 4 of Sharper. Comparator 70 first compares the eighth bit (Xth bit) "from two frames earlier and four frames earlier which were stored in the register 142" (Sharper -- col.

8, lines 6-7). Only if both of the eighth bits have been converted (i.e., represented as an off-hook or maintenance system mode) will the first stage output 66 equal a logic 1 (Sharper -- col. 8, lines 8-11). The output 66 is then fed into the second stage of comparator 70, with the gating signal on line 65 forcing the second stage output to be a logic 1, except when the eighth bit of any byte is selected by the shift register 142 (Sharper -- col. 8, lines 13-27). The third stage of comparator 70 compares the eighth bit on line 40 for each byte per frame to the prior eighth bit from two frames earlier and four frames earlier, and places the resulting comparison on the output signal 72 (Sharper -- col. 8, lines 29-50). Accordingly, the truth table shown in Fig. 5b of Sharper notes that whenever the previous frames (two frames earlier and four frames earlier) yield a logic 1 value, then it is known the system is operating in maintenance mode since alternating frames, eighth bit location, is in a logic 1 state (Sharper -- Fig. 5b, lines 61, 62). However, the current eighth bit (line 40) of the current frame is two frames and four frames after the logic values at lines 61 and 62, respectively. Given that the current eighth bit is now different from the preceding two frames and four frames, Sharper teaches that the current frame must be restored on the output 72. That restoration on output 72 will be opposite the converted state of logic 1 (Sharper -- col. 8, lines 8-11).

It is known that Sharper teaches comparison. The comparison register can be equated to register 142 (Sharper -- Fig. 4). Register 142 stores a first signal bit received over a voice channel 61 (Sharper -- Fig. 4). A comparator 70 compares signal 61 as the first signal bits against second signal bits 62, also contained within register 142 and received over a voice channel. However, this is where the similarity ends between Sharper and present claims 10 and 18. While signals 61 and 62 can be compared with each other, the comparison outcome does not dictate that the logic value within successive eighth bit frames of signal 61 be replaced by the logic value of eighth bit frames of signal 62. In fact, the two frames prior and four frames prior eighth bits are never changed, and certainly the logic value of signal 61 is not replaced by that of signal 62. Sharper does not teach going back in time and changing, restoring, or in any way manipulating a prior sequence of signal bits. Instead, the only significance to Sharper is that the current eighth bit can be restored to its pre-converted state, that eighth bit being what is received on line 40 (Sharper -- Fig. 4). The current eighth bit is restored based on its comparison to the two frames prior and four frames prior eights bits coming in as signals 61 and 62, respectively.

If the Examiner is alleging that the later-in-time eighth bit (current eighth bit) being restored based on the status of the prior eighth bit frames is the same as that claimed in present claims 10 and 18, Appellants respectfully disagree. Restoring the current eighth bit based on its comparison to the prior eighth bit is exactly the opposite of that which is claimed. Claims 10 and 18 specifically replace the prior bit sequence (first signal bits) with the subsequent bit sequence (second signal bits) if the second bit sequence is different from the first. Sharper, however, specifically does not change either the first bit sequence (61) or the second bit sequence (62) regardless of any comparison.

The shortcomings of Sharper are compounded in Robertson. Robertson makes no mention whatsoever of replacing first signal bits with second signal bits. Instead, Robertson only describes detection of any occurrence of matches. Detection is not the same as replacement, and certainly would not be interpreted to be the same by a skilled artisan.

Sharper and Roberson do not teach or suggest a comparator that notifies a digital signal processor of a replacement. Present claim 10 not only describes a comparator that replaces first signal bits with second signal bits, but also a comparator that notifies a digital signal processor (DSP) of that replacement. In this fashion, the DSP need only be notified if a change exists. If a change does not occur, then the DSP is not bothered using standard interrupts or any other process halting function.

Contrary to present claim 10, Sharper makes no mention of any notification to a DSP as recognized by the Examiner on page 2 of the Office Action. However, the Examiner believes that Robertson describes a system for notifying a DSP. The Examiner points to member 882 in Robertson for performing a comparison and the result of that comparison is then somehow forwarded to a DSP (Office Action -- page 2). Applicants respectfully disagree. First, the comparator function 882 has no means whatsoever for communicating the comparison output to a processor since all functional arrows extend inward to comparator 882, not outward from comparator 882 (Robertson -- Fig. 12). Thus, the comparator apparatus 882 cannot signal anything whatsoever to a DSP through processor buffer 805 or otherwise. Second, even if comparator 882 could hypothetically forward a signal to a DSP, it only determines an occurrence

of matches (Robertson -- col. 16, lines 51-55). Nowhere in Robertson is there any mention that comparator apparatus 882 does anything other than determining the occurrence of matches "in combination with instruction of central processor origin and signals from detectors 815-817 . . ." (Robertson -- col. 16, lines 53-55). Determining the occurrence of matches is quite different from notifying a DSP of a replacement as presently claimed.

For at least the reasons set forth above, Appellants believe independent claims 10 and 18 are patentably distinct over the cited art, both singularly and in combination.

Rejection of Claims 11-17 and 19-23

Claims 11-17 and 19-22 [sic] stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sharper, Robertson, and U.S. Patent No. 6,782,066 to Nicholas et al. (hereinafter "Nicholas"). Although pending, the Examiner does not specifically address claim 23 in the Office Action. Moreover, no explanation is given as to why or how the system of Nicholas could be combined with that of Sharper and/or Robertson to arrive at the present claims. Accordingly, Appellants believe dependent claims 11-17 and 19-23 are patentably distinct over the cited references, both singularly and in combination, for at least the same reasons as their respective base claim discussed above.

* * *

For the foregoing reasons, it is submitted that the Examiner's rejection of and objection to pending claims 10-23 was erroneous, and reversal of the Examiner's decision is respectfully requested.

The Commissioner is hereby authorized to charge the required fee(s) or credit any overpayment to LSI Logic Corporation deposit account number 12-2252.

Respectfully submitted,

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Date: June 26, 2007
KLD

VIII. APPENDIX

The present claims on appeal are as follows.

10. A telephony signaling circuit, comprising:

a comparison register adapted to store first signal bits contained within a first data sequence received over a voice channel; and

a comparator adapted to compare the first signal bits stored in the comparison register against second signal bits contained within a second data sequence received over the voice channel and, if the first signal bits differ from the second signal bits, to replace the first signal bits stored in the comparison register with the second signal bits and to notify a digital signal processor coupled to the comparator of the replacement.

11. The telephony signaling circuit as recited in claim 10, further comprising a modification register adapted to store third signal bits, and a data modifier adapted to place the stored third signal bits into a third data sequence and to subsequently transmit the third data sequence over the voice channel.

12. The telephony signaling circuit as recited in claim 11, further comprising multiple voice channels, such that each voice channel is adapted to receive a plurality of data sequences, each of which contains a unique combination of signal bits, and wherein one of a plurality of comparison registers, data comparators, modification registers and data modifiers is associated with each voice channel.

13. The telephony signaling circuit as recited in claim 12, wherein in response to being notified by the data comparator of the replacement of the signal bits in the comparison register, the DSP changes, during use, the status of the respective voice channel.

14. The telephony signaling circuit as recited in claim 12, wherein the DSP is configured to change the third signal bits stored in the modification register and cause the data modifier to place the changed third signal bits into a data sequence and to subsequently transmit the data sequence over the voice channel.

15. The telephony signaling circuit as recited in claim 12, wherein the received and transmitted data sequences comprise time division multiplexed voice data, as typically used for telephone communication.

16. The telephony signaling circuit as recited in claim 12, further comprising a packet control processor (PCP) adapted to receive notification from the comparator of a change in the first signal bits stored in the comparison register, and to change third signal bits stored in the modification register.

17. The telephony signaling circuit as recited in claim 16, wherein receiving notification from the comparator comprises receiving a hardware interrupt issued by the comparator.

18. A method for detecting telephony signals, comprising:

storing in a comparison register first signal bits contained within a first data sequence received over an input voice channel;

comparing the first signal bits against second signal bits contained in a second data sequence received over the input voice channel; and

if the first signal bits differ from the second signal bits, replacing the first signal bits with the second signal bits.

19. The method as recited in claim 18, further comprising storing third signal bits in a modification register, using a data modifier to place the stored third signal bits into a third data sequence and subsequently transmitting the third data sequence over an output voice channel.

20. The method as recited in claim 18, further comprising multiple input voice channels, such that each input voice channel is adapted to receive a plurality of data sequences, each of which contains a unique combination of signal bits, and wherein one of a plurality of comparison registers, data comparators, modification registers and data modifiers is associated with each input voice channel.

21. The method as recited in claim 18, further comprising multiple output voice channels, such that each output voice channel is adapted to transmit a data sequence containing a unique combination of signal bits, and wherein one of a plurality of modification registers and data modifiers is associated with each output voice channel.

22. The method as recited in claim 18, further comprising notifying a processor if the first signal bits differ from the second signal bits.

23. The method as recited in claim 19, further comprising the processor, upon being notified that the first signal bits differ from the second signal bits, changing the third signal bits stored in the modification register and causing the data modifier to place the changed third signal bits into the third data sequence, and subsequently transmit the third data sequence over the output voice channel.

IX. EVIDENCE APPENDIX

No evidence has been entered during the prosecution of the captioned case.

X. RELATED PROCEEDINGS APPENDIX

No prior or pending appeals, interferences, or judicial proceedings are known to Appellant or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.